REMARKS

Entry of this response is proper under 37 CFR §1.116, since no new claims or issues are raised and the Examiner is respectfully requested to clarify the rejection of record prior to proceeding to Appeal, since the rejection currently of record fails to indicate which layers in the cited reference is considered to correlate with the layers described in the claimed invention.

Furthermore, since the latest Office Action fails to clarify the rejection of record sufficient for Applicants to properly prepare for Appeal, Applicants request that the finality of the rejection be withdrawn as premature, since the rationale of the rejection is not at all clear either from the rejection itself or from the Examiner's Response on page 2 of the Office Action.

As best understood, claims 1-9 and 16-20 are all the claims presently pending in the application. Claims 10-15 stand withdrawn resultant from restriction but are subject to evaluation for rejoinder upon ultimate determination of allowable subject matter. It is noted that the rejection of record contradicts itself by indicating claim 10 to withdrawn (per item 6 on Office Action Summary page) as well as rejected (see rejection on page 3 of Office Action).

It is noted that the claim amendments, if any, are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-10 and 16-20 nominally stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over US Patent 6,642,539 to Ramesh et al.

This rejection based on Ramesh, as best can be deciphered, is respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described, for example, in independent claim 1, the claimed invention is directed to a storage medium including a metallic underlayer, a ferroelectric data layer over the metallic underlayer, and a layer over the ferroelectric data layer having a charge migration rate faster than a charge migration rate of the ferroelectric data layer.

As explained at lines 11-17 of page 2 of the specification, no solution has yet been found to the surface depolarization problem that plagues the art of ferroelectric disk technology using vertical polarization of an FE surface, as explained in more detail beginning at line 22 on page 6, wherein is described a slow loss of surface polarization over several to 24 hours time scale. The inventors recognized that this effect was due not to loss of bulk polarization in the FE film but to accumulation of mobile surface charges which neutralize the bound charges constituting the surface polarization.

The claimed invention provides a solution to the surface polarization by providing a layer over the ferroelectric data layer that has a charge migration rate that is faster than the charge migration rate of the ferroelectric data layer.

II. THE PRIOR ART REJECTION

The Examiner alleges that newly-cited Ramesh renders obvious the present invention as defined by claims 1-10 and 16-20. Applicants again respectfully disagree and again respectfully submit that the rejection of record fails to establish a *prima facie* rejection either for anticipation or for obviousness, at least, not until the Examiner provides positive identification as to which layers in Ramesh are being relied upon to demonstrate the claimed invention.

Applicants first note that the principle of operation of the memory of the present invention is very different from that described in Ramesh, in spite of some similarities in materials. The memory of Ramesh relates to a capacitor/transistor cell structure such as shown in Figure 1.

In contrast, the memory unit of the present invention is not based upon any form of capacitor/transistor cell structure in the memory cell area. Instead, the technology of the present invention provides a much higher density technology wherein a bit of data is stored in a cell size approaching a nanometer, using ferroelectric dipoles (e.g., polarized domains) within the ferroelectric medium itself. This newer technology is expected to yield density capable of 3000 Gb/in^2, which would be orders of magnitude higher than the density achievable using capacitor/transistor structures such as demonstrated by Ramesh.

In the rejection currently of record, the Examiner points to Figure 8 of Ramesh, along with the description at lines 14-23 of column 9.

However, Applicants remain completely baffled as to exactly what the Examiner is attempting to assert in this rejection, since Figure 8 is described at lines 33-34 of column 13

as being an alternate configuration for the gate dielectric layer 16 of Figures 1, 5, and 7. As such, it would seem to have very little relation to the claimed invention, absent additional clarification by the Examiner.

Turning to the Examiner's Response to Arguments on page 2 of the Office Action, as best can be deciphered, the Examiner's position is based upon considering the layer 66 (e.g., the PZT layer) as being the ferroelectric data layer. Therefore, as best can be deciphered, the Examiner would have to consider the LSCO layers 64, 68 as corresponding to the metallic underlayer and the layer having the charge migration rate faster than that of the ferroelectric data layer PZT 66, as the additional elements of the independent claims.

However, in exemplary embodiments of the claimed invention, the metallic underlayer is exemplarily described in claim 7 as comprising $SrRuO_3$, and the faster charge migration layer is exemplarily described in claim 4 as comprising silicon and/or a doped perovskite.

Therefore, contrary to the Examiner's characterization, there does not appear to be any possible demonstration of the claimed structure in Figure 8 of Ramesh, since the two layers adjacent to the PZT layer 66 are both LSCO (described in lines 23-24 of column 12 as being $La_{1-x}Sr_xCoO_3$) and the Examiner fails to demonstrate that this structure satisfies the plain meaning of the description of the independent claims.

As Applicants pointed out in their previous response, the mere presence of having one or more similar materials present in Ramesh fails to establish a *prima facie* rejection, since the claimed invention is not merely reciting materials but includes a precisely defined structure. This structure is clearly not demonstrated by Figure 8 of Ramesh.

As Applicants also explained in their previous response and as explained in lines 11-13 of page 2 of the disclosure, the underlying principles of operation of the present invention includes that of using ferroelectric bits that are on the order of one nanometer. This concept of bit storage is entirely different from the technology described in Ramesh, which relies upon storage cells comprising transistor structures 12-18 shown in Figures 1, 5, 7, and 9 of this reference.

In contrast to Ramesh, as exemplarily shown in Figure 1 of the present application, the present invention stores bits of information as very localized portions of polarization of a ferroelectric data layer (e.g., FE DL, 101), using vertical polarization (e.g., an electric field normal to the disk surface) as the mechanism to write data. As explained in lines 19-20 of page 6, as of the filing date, the inventors had been able to achieve the capability to write

patterns on the scale of 1000 Å, a density considerably greater than that possible using transistor-based memory cells such as used in Ramesh.

As explained at lines 20-21 of page 6, the problem being addressed by the present invention is that the inventors recognized there to be a slow surface depolarization of the polarization-written information. As explained at the top of page 7, the inventors were able to discover that this slow loss of surface polarization was not due to a loss of bulk polarization in the FE film, but, rather, was due to accumulation of mobile surface charges which neutralize the bound charge constituting the surface polarization.

The solution offered by the present invention is that of providing an overlying conducting layer (e.g., layer 211 shown in Figure 2), thereby shielding against this depolarization.

Therefore, the type of ferroelectric memory of the present invention is entirely different from the ferroelectric memory cell used in Ramesh, even if there are some co-incidental similarities in some materials. That is, there is nothing in Ramesh that corresponds to the structure 210 shown in Figure 2 of the present application and as described in the independent claims, and the Examiner makes no attempt in the rejection of record to point out such corresponding structure in Ramesh. Absent such demonstration of corresponding structure, the rejection clearly fails to establish a *prima facie* rejection.

Along this line, it is noted that the "broadest reasonable interpretation" of any disputed claim terminology must be consistent with the description in the disclosure of the application under evaluation, as clearly explained in the first sentence of MPEP §2111: "*During patent examination, the pending claims must be given their broadest reasonable interpretation consistent with the specification.*" (emphasis by Applicants)

Therefore, contrary to the implication in the rejection currently of record, merely identifying common materials in the prior art reference does not provide any indication of equivalent structure and/or inherency to the claimed invention, if for no other reason that the underlying technology and structure of Ramesh is completely different from (e.g., inconsistent with) that described by the specification of the present application.

Hence, turning to the clear language of the claims, in Ramesh there is no teaching or suggestion of: "*A storage medium, comprising: a metallic underlayer; a ferroelectric data layer over said metallic underlayer; and a layer over said ferroelectric data layer having a charge migration rate faster than a charge migration rate of said ferroelectric data layer*", as required by independent claim 1. The remaining independent claims have similar language.

Therefore, Applicants again respectfully submit that there are features of the claimed invention that are not taught or suggested by Ramesh, and the Examiner is respectfully requested to reconsider and withdraw this rejection based on Ramesh.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-9 and 16-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance, and that withdrawn claims 10-15 are also in condition to be rejoined and allowed. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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